VLSI Design (BEC-41)
(Unit-2, Lecture-7)

Presented By:

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MOS Combinational Circuit

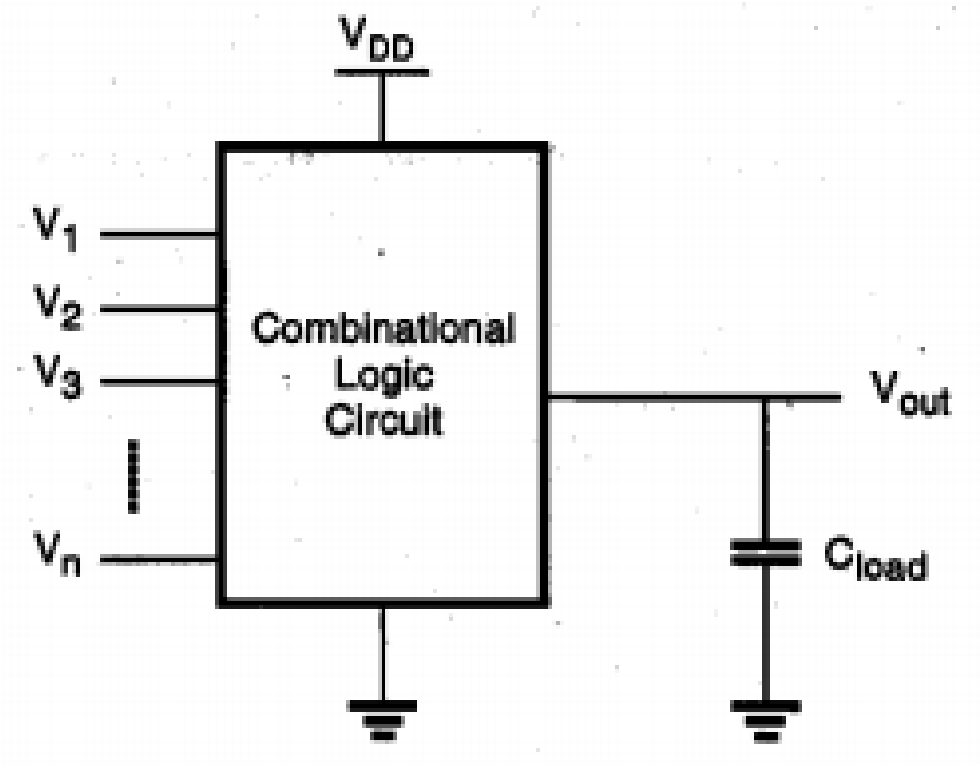


Fig. Generic combinational logic circuit (gate).

- Combinational logic circuits, or gates, which perform Boolean operations on multiple input variables and determine the outputs as Boolean functions of the inputs, are the basic building blocks of all digital systems.
- In this chapter, we will examine the static and dynamic characteristics of various combinational MOS logic circuits.

MOS Combinational Circuit

CMOS NOR2 (Two-Input NOR) Gate

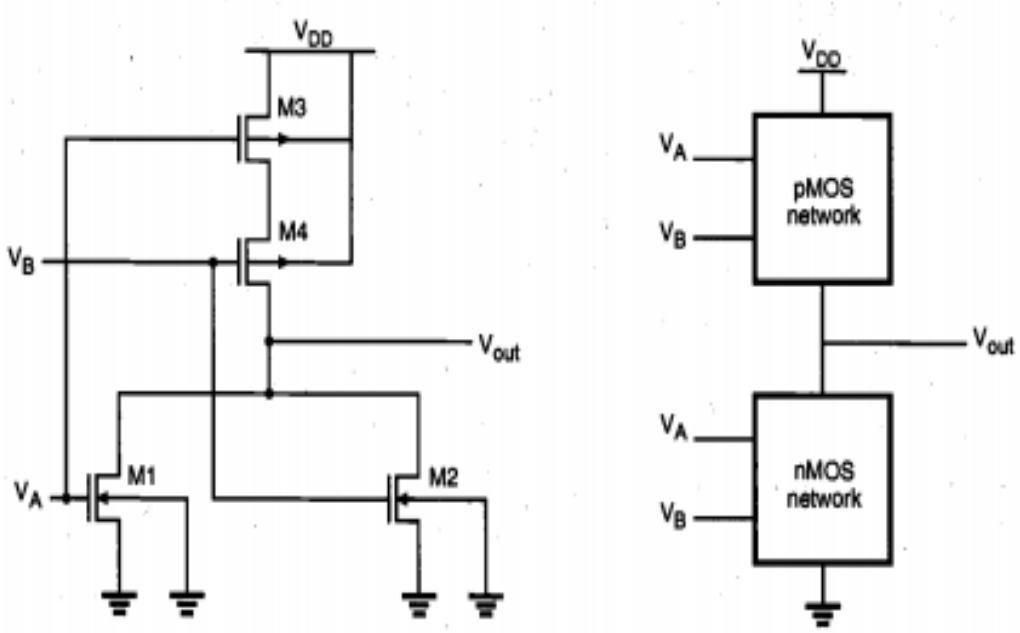


Fig. (Two-Input NOR) Gate.

- The output voltage of the CMOS NOR gate will attain a logic-low voltage of $V_{OL} = 0$ and a logic-high voltage of $V_{OH} = V_{DD}$.
- For circuit design purposes, the switching threshold voltage Vth of the CMOS gate emerges as an important design criterion.
- We start our analysis of the switching threshold by assuming that both input voltages switch simultaneously, i.e., $V_A = V_B$.

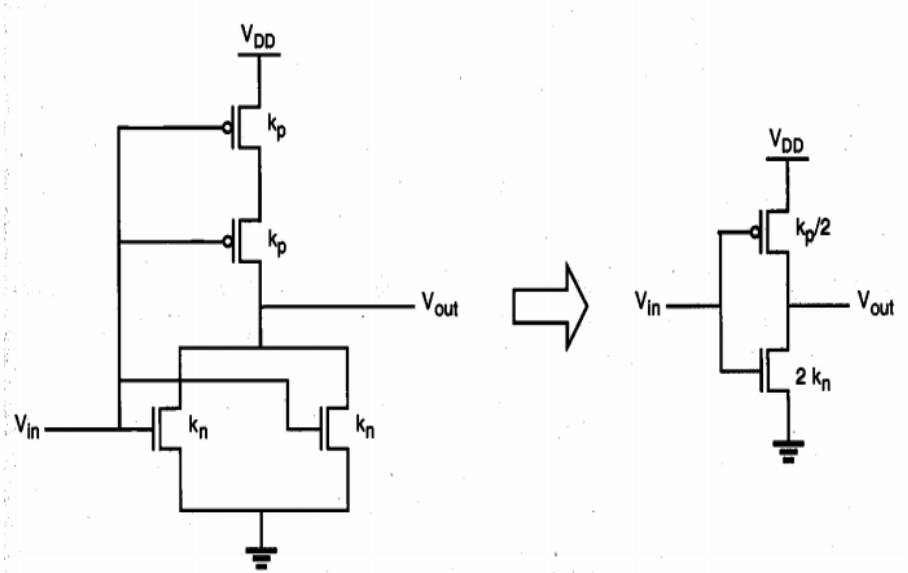
MOS Combinational Circuit

CMOS NOR2 (Two-Input NOR) Gate

- The switching threshold by assuming that both input voltages switch simultaneously, i.e., $V_A = V_B$.

$$V_{th}(\text{NOR2}) = \frac{V_{T,n} + \sqrt{\frac{k_p}{4k_n}}\left(V_{DD} - |V_{T,p}|\right)}{1 + \sqrt{\frac{k_p}{4k_n}}}$$

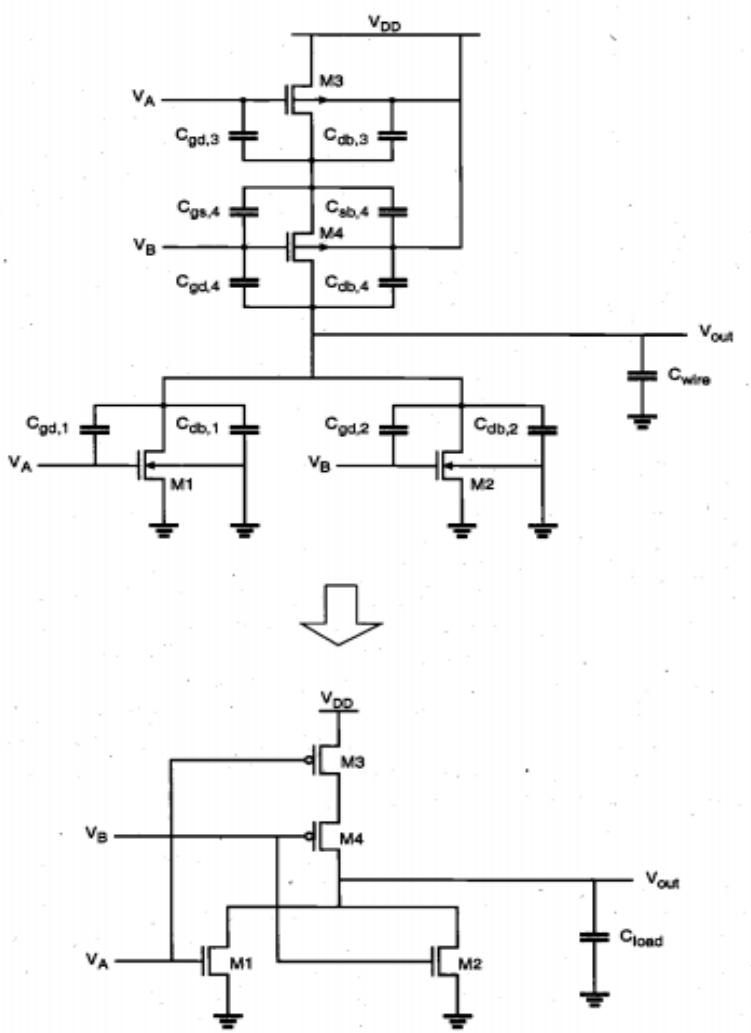
- we can easily derive simple design guidelines for the NOR2 gate. For example, in order to achieve a switching threshold voltage of $V_{DD}/2$ for simultaneous switching, we have to set $V_{T,n} = |V_{TP}|$ and $k_p = 4\ k_n$.



MOS Combinational Circuit

CMOS NOR2 (Two-Input NOR) Gate

- The CMOS NOR2 gate with the parasitic device capacitances, the inverter equivalent, and the corresponding lumped output load capacitance.
- In the worst case, the total lumped load capacitance is assumed to be equal to the sum of all internal parasitic device capacitances seen in Figure.



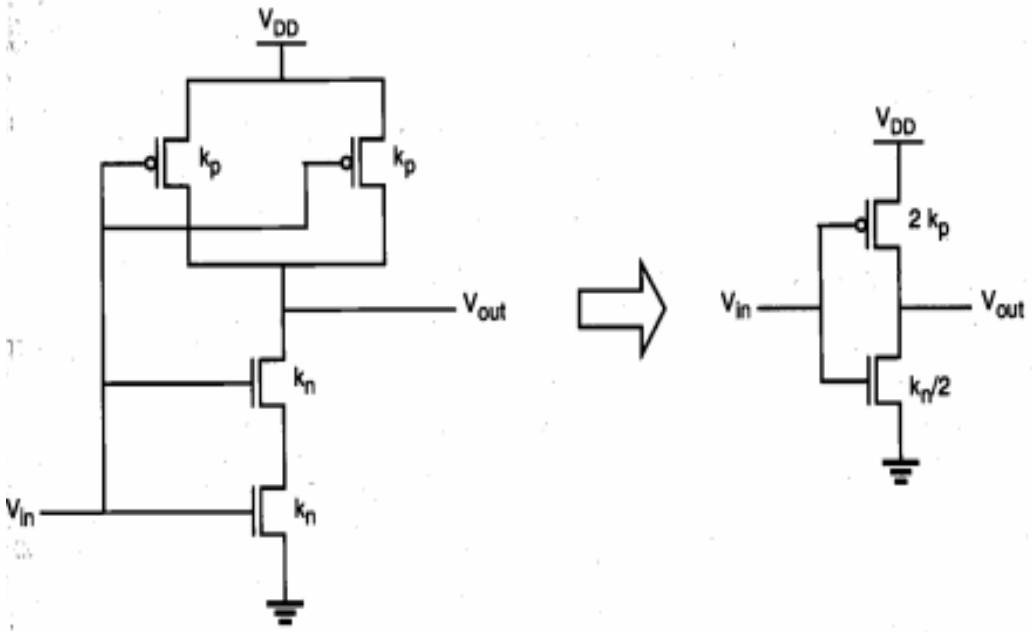
MOS Combinational Circuit

CMOS NAND2 (2-Input NAND) Gate

- The operating principle of this circuit is the exact dual of the CMOS NOR2 operation examined earlier.
- The n-net consisting of two series-connected NMOS transistors creates a conducting path between the output node and the ground only if both input voltages are logic-high, i.e., are equal to V_{OH}.
- In this case, both of the parallel-connected PMOS transistors in the p-net will be off.
- For all other input combinations, either one or both of the PMOS transistors will be turned on, while the n-net is cut-off, thus creating a current path between the output node and the power supply voltage.

MOS Combinational Circuit

CMOS NAND2 (2-Input NAND) Gate



- A switching threshold voltage of $V_{DD}/2$ (for simultaneous switching) is achieved by setting $V_{T,n} = |V_{T,p}|$ and $k_n = 4k_p$ in the NAND2.

- Using an analysis similar to the one developed for the NOR2 gate, we can easily calculate the switching threshold for the CMOS NAND2 gate. Again, we will assume that the device sizes in each block are identical, with $(W/L)_{n,A} = (W/L)_{n,B}$ and $(W/L)_{P,A} = (W/L)_{p,B}$.
- The switching threshold for this gate is then found as

$$V_{th}(\text{NAND2}) = \frac{V_{T,n} + 2\sqrt{\frac{k_p}{k_n}}\left(V_{DD} - |V_{T,p}|\right)}{1 + 2\sqrt{\frac{k_p}{k_n}}}$$

MOS Combinational Circuit

CMOS NAND2 (2-Input NAND) Gate

- This figure shows the CMOS NOR2 gate with the parasitic device capacitances, the inverter equivalent, and the corresponding lumped output load capacitance.
- In the worst case, the total lumped load capacitance is assumed to be equal to the sum of all internal parasitic device capacitances seen in Figure.