

## HOW TO APPLY/REGISTER

Registration Start Date	02/05/2026
Last Date of Registration	24/05/2026
Last date of deposition of fees	24/05/2026
Commencement of Training Program	01/06/2026

The students can enroll in internship program either for six weeks or four weeks, therefore fee should be paid accordingly through online mode. Registration charges are non-Refundable. Online registration can be done in following three steps: -

**Step 1:** Register by going through the following links or by scanning QR code.

<https://forms.gle/CAT7KWf49q5eSxCY6>

**Step 2:** Fill the google form and upload the required documents.

**Step 3:** Submit the google form.

**Note:** Separate charge as per university norms will be applicable if any student is allowed for hostel accommodation during internship period only on the availability of seats.

### Eligibility:

Students of various institutions comprising of **Diploma/ B.Tech / M.Tech / MSc /PhD to register.**

### Account Details.

**Account No.:** 33542824744

**IFSC Code:** SBIN0002578

**Account Name:** Madan Mohan Malaviya University of Technology.

**Bank Name:** State Bank of India

## COURSE FEE

Fee Type	Registration Fee
Six/Four Weeks (Students)	3000/2000 INR

## AWARDS

The participants who have completed a minimum of 75% attendance will be given "Successful Completion Certificate".

## SPEAKERS/INSTRUCTORS

- Prof. R. K. Chauhan, ECED, MMMUT, Gkp,
- Dr. Alok Kumar Shukla, ECED, MMMUT, Gkp,
- Mr. Prashant Pandey, EED, REC, Sonbhadra,
- Dr. Narendra Yadava, ECED, DDUGU, Gkp,
- Dr. Mangal Deep Gupta, ECED, BBAU, Lko,
- Ms. Shweta Yadava, ECED, MMMUT, Gkp,
- Mr. Kuldip Kannaujiya, ECED, MMMUT, Gkp,
- Mr. Prashant Pandey, ECED, MMMUT, Gkp,
- Ms. Kanchan Lata Srivastava, ECED, MMMUT Gorakhpur.

## REGISTER HERE

SCAN HERE



## CONTACT US

**Mr. Kuldip Kannaujiya (7355721453)**

[2025048007@mmmud.ac.in](mailto:2025048007@mmmud.ac.in)

**Mr. Prashant Pandey (8077848965)**

[2025048020@mmmud.ac.in](mailto:2025048020@mmmud.ac.in)

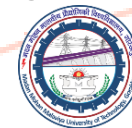
**Ms. Kanchan Lata Srivastava (9696818004)**

[2025048019@mmmud.ac.in](mailto:2025048019@mmmud.ac.in)

## Summer Internship on VLSI Devices to Systems Design using Silvaco, Cadence and FPGA (VSDSCF-2026)

June-July 2026

Organized By



VLSI DESIGN LAB,  
Centre of Excellence  
DEPARTMENT OF ELECTRONICS AND  
COMMUNICATION ENGINEERING  
Chips to Startup (C2S) MeitY  
**MADAN MOHAN MALAVIYA  
UNIVERSITY OF TECHNOLOGY,  
GORAKHPUR (UP)**

### Patron

**Prof. J. P. Saini**

Vice Chancellor  
MMMUT, Gorakhpur

### Chairman & Principal Coordinator

**Prof. S. K. Soni**

HOD, Electronics and Communication  
Engineering, MMMUT, Gorakhpur

**Prof. R. K. Chauhan**

PI, Electronics and Communication  
Engineering, MMMUT, Gorakhpur

### Coordinator

**Dr. Alok Shukla**

Assistant Professor, Electronics and  
Communication Engineering,  
MMMUT, Gorakhpur

**Mr. Prashant Pandey**

Assistant Professor, Electronics  
Engineering, REC, Sonbhadra

# ABOUT SCHEDULED EVENTS

## ATLAS

1.	Introduction to TCAD
2.	Overview of Silvaco TCAD Tools
3.	Introduction to Atlas Device Simulator
4.	Basic Simulation Flow in Atlas
5.	Structure Definition & Meshing
6.	Physical Models & Boundary Conditions
7.	Biasing and Simulation Execution.
8.	Introduction to TonyPlot Tool
9.	MOSFET Simulation using Atlas (Practical)
10.	Result Analysis & Performance Comparison

## CADENCE

1.	Introduction to Cadence Tools
2.	Overview of Cadence Design Environment
3.	Schematic Design using Virtuoso
4.	Symbol Creation & Library Management
5.	Analog Circuit Design Basics
6.	Introduction to Simulation (ADE)
7.	DC, AC & Transient Analysis
8.	Layout Design using Virtuoso Layout
9.	DRC & LVS Verification
10.	Layout Simulation & Result Analysis

## FPGA

1.	Introduction to FPGA
2.	Overview of FPGA Architecture
3.	Introduction to HDL (Verilog/VHDL)
4.	Design Entry using HDL Coding
5.	Simulation of Digital Circuits
6.	Synthesis Process in FPGA
7.	Implementation (Mapping, Placement & Routing)
8.	Timing Analysis & Constraints
9.	FPGA Programming & Hardware Testing
10.	Mini Project Implementation on FPGA