VLSI Design (BEC-41)
(Unit- 2, Lecture- 9)

Presented By:

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Problem 1: Design following Boolean expression using complementary CMOS and Pseudo NMOS logic:

$$Y = \overline{AB + C(A + D)} \quad Y = AB + BC + D.$$

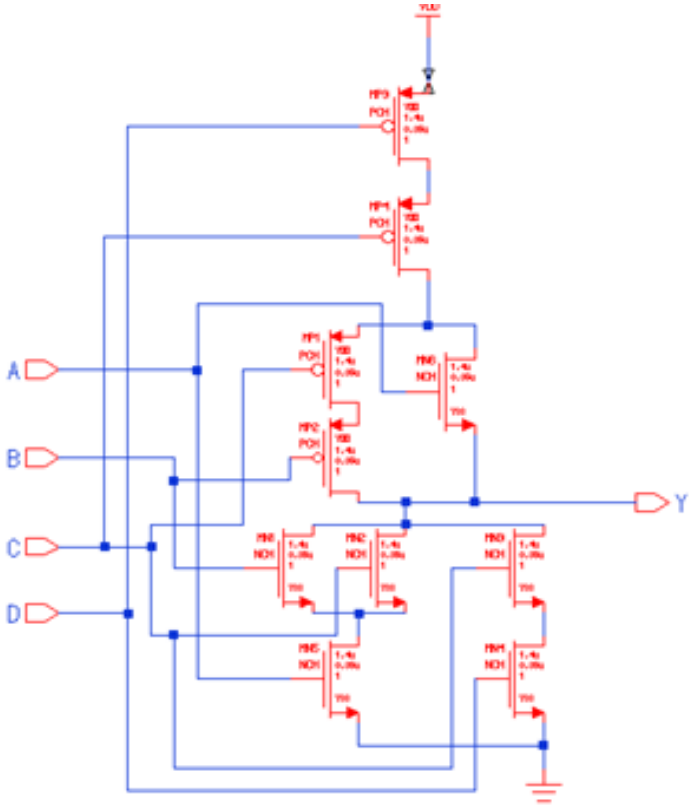


Fig. using complementary CMOS logic

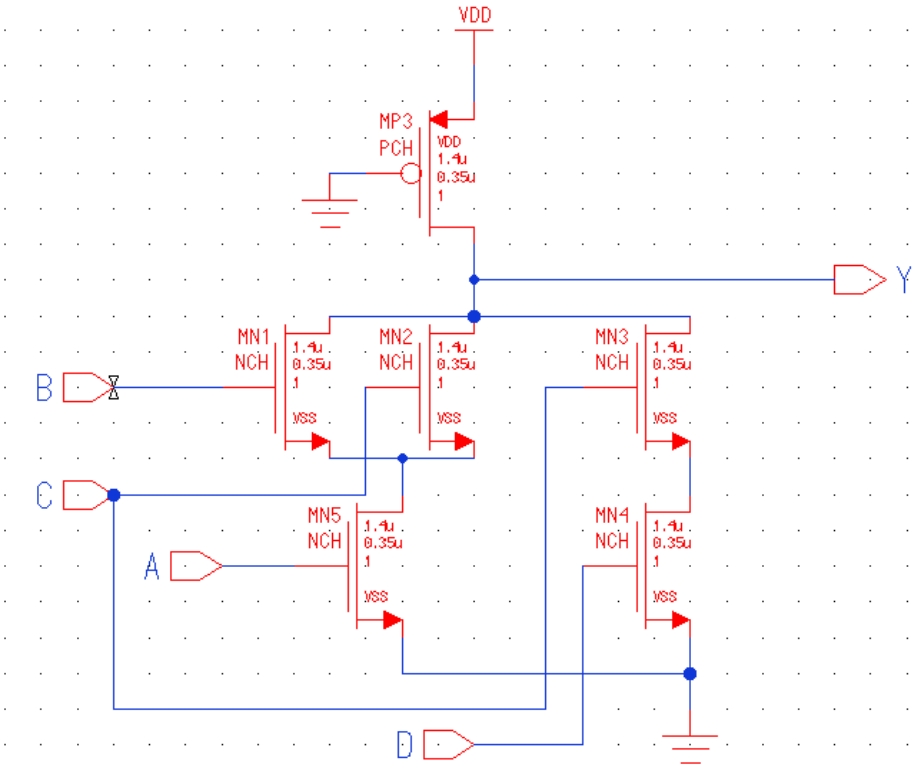
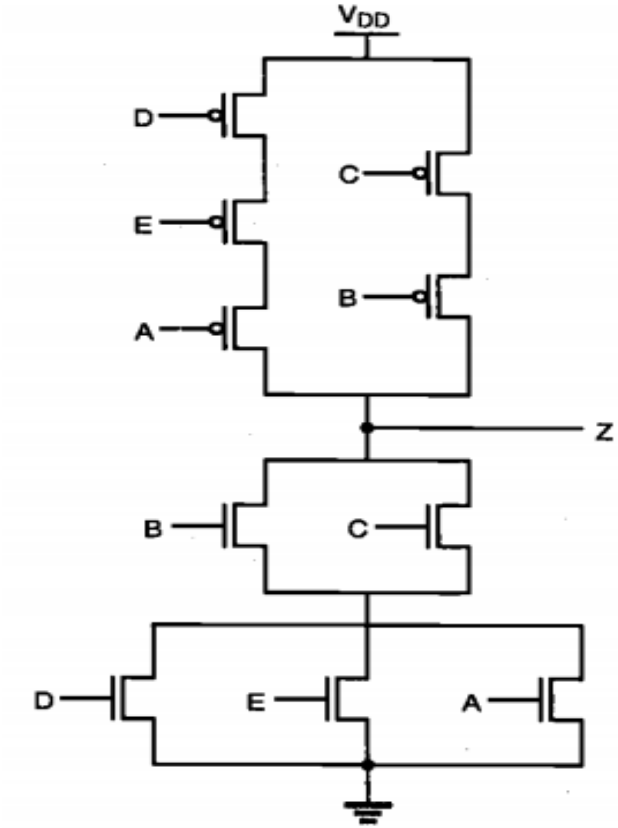


Fig. using Pseudo NMOS logic

Problem 2: **Realized following Boolean function and find (W/L)n equivalent and (W/L)p equivalent, if (W/L)n=10 and (W/L)p=15:**

$$Y = \overline{(\boldsymbol{D} + \boldsymbol{E} + A)(\boldsymbol{B} + \boldsymbol{C})}$$



$$\left(\frac{W}{L}\right)_{n,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E + \left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{30} + \frac{1}{20}} = 12$$

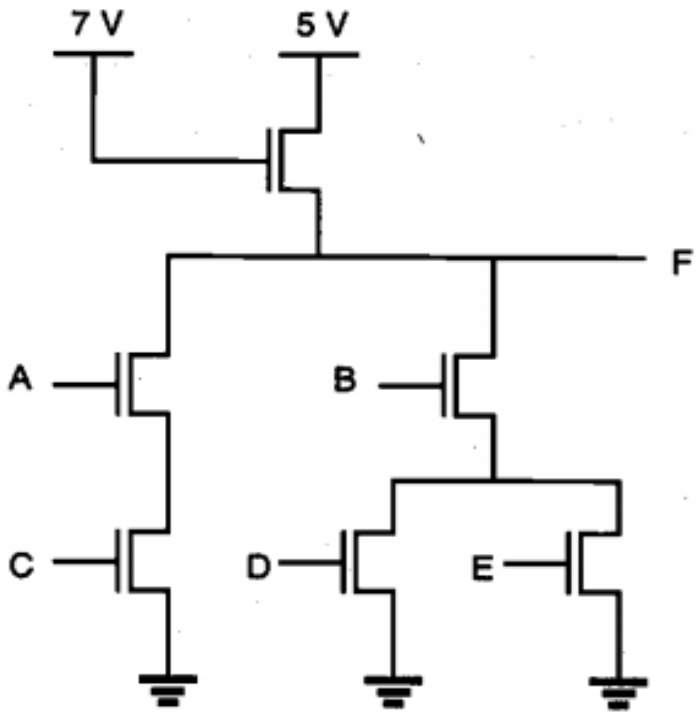
$$\left(\frac{W}{L}\right)_{p,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D} + \frac{1}{\left(\frac{W}{L}\right)_E} + \frac{1}{\left(\frac{W}{L}\right)_A}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} + \frac{1}{\frac{1}{15} + \frac{1}{15}} = 12.5$$

Problem 2:

A. Identify the worst-case input combination(s) for V_{OL}.

B. Calculate the worst-case value of V_{OL}. (Assume that all pull-down transistors have the same body bias and initially, that V_{OL} =5% V_{DD}.)



Solution 2:

Class1: A-C

Class1: B-D

Class1: B-E

Class2: B-D-E

Class3: A-C-B-D-E

$V_{OL1}>V_{OL2}>V_{OL3}$

Hence worst case V_{OL} in class 1 combination.

Given: $R_n/(R_u+R_n).\ V_{DD} = 5\%V_{DD} = V_{DD}/20$

Hence $19R_n = R_u$

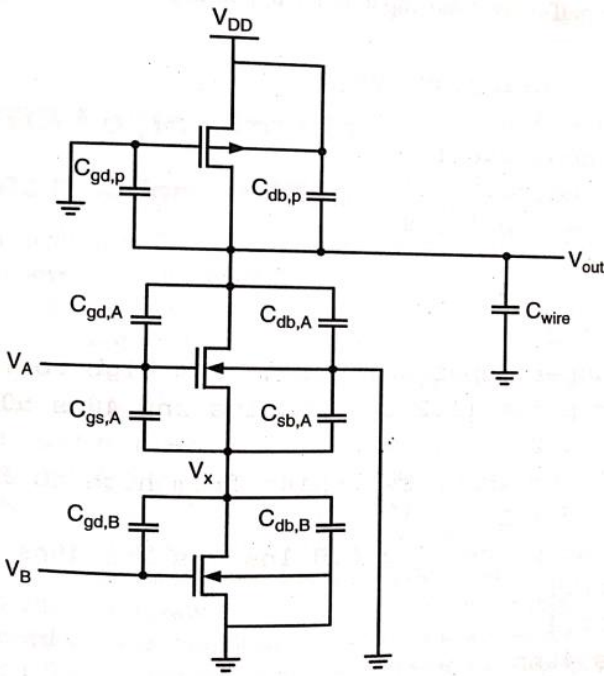
For Class1: $V_{OL} = 2R_n/(R_u+2R_n).\ V_{DD}$

$V_{OL} = V_{DD}/10.5$

Problem 3: **Find the effective output node capacitance in both two cases of given figure:**

A. The input VA is equal to V_{OH} and the other input V is switching from V_{OH} to V_{OL}.

B. V_B is equal to V_{OH} and V_A switches from V_{OH} to V_{OL}.



Solution 3:

- The input V_A is equal to V_{OH} and the other input V is switching from V_{OH} to V_{OL}. In this case, both the output voltage V_{OUT}, and the internal node voltage V_x will rise, resulting in:

$$C_{load} = C_{gd,load} + C_{gd,A} + C_{gd,B} + C_{gs,A} + C_{db,A} + C_{db,B} + C_{sb,A} + C_{sb,load} + C_{wire}$$

- Note that this value is quite conservative and fully reflects the internal node capacitances into the lumped output capacitance C_{load} in reality, only a fraction of the internal node capacitance is reflected into C_{load}.
- Now consider another case where V_B is equal to V_{OH} and V_A switches from V_{OH} to V_{OL}. In this case, the output voltage V_{out}, will rise, but the internal node voltage V_x, will remain low because the bottom driver transistor is on. Thus, the lumped output capacitance is

$$C_{load} = C_{gd,load} + C_{gd,A} + C_{db,A} + C_{sb,load} + C_{wire}$$