Addressing Modes

- Various ways of specifying the operands or various formats for specifying the operands is called addressing mode
- 8-bit or 16-bit data may be directly given in the instruction itself
- The address of the memory location, I/O port or I/O device, where data resides, may be given in the instruction itself
- In some instructions only one register is specified. The content of the specified register is one of the operands. It is understood that the other operand is in the accumulator.

- Some instructions specify one or two registers. The contents of the registers are the required data.
- In some instructions data is implied. The most instructions of this type operate on the content of the accumulator

Addressing Modes (8085)

- Implicit addressing
  - CMA – Complement the contents of accumulator
- Immediate addressing
  - MVI R, 05H
  - ADI 06H
- Direct addressing – The address of the operand in the instruction - STA 2400H, IN 02H

- Register addressing
  - In register addressing mode the operands are in the general purpose registers
  - MOV A, B
  - ADD B
- Register indirect addressing
  - Memory location is specified by the contents of the registers
  - LDAX B, STAX D, MOV A,M

Instructions of 8085

Data Transfer Instructions

Types	Examples
1. Between Registers	1. MOV B,D – Copy the contents of the register B into Register D
2. Specific data byte to a register or a memory location	2. MVI B,32H – Load register B with the data byte 32H
3. Between a memory location and a register	3. LXI H, 2000H MOV B,M From a memory location 2000H to register B
4. Between an I/O device and the accumulator	4. IN 05H – The contents of the input port designated in the operand are read and loaded into the accumulator

MOV: This instruction copies the contents of source register into destination register.

- MOV Rd,Rs
- MOV M,Rs
- MOV Rd,M

These instructions are 1 byte instructions.

Examples: MOV A,B

MOV B,M

MOV M,A

Flags: No flags are affected

If one of operands is memory location, it is specified by HL pair register.

Opcode	Operand	Byte	M- Cycle	T-State
MOV	Rd, Rs	1	1	4
MOV	M, Rs	1	2	7
MOV	Rd, M	1	2	7

MVI R,8 bit data: Store 8 bit data in destination register or memory. If destination is memory, it is specified by the HL pair register.

Opcode	Operand	Byte	M- Cycle	T-State
MVI	R, Data	2	2	7
MVI	M,Data	2	3	10

No flags are affected.

LXI Rp/SP, 16 bit data: Loads 16 bit data in register pair/stack pointer.

Opcode	Operand	Byte	M- Cycle	T-State
LXI	Rp, Data(16)	3	3	10
LXI	SP,Data(16)	3	3	10

- **No flags are affected.**
- **Second byte of instruction specifies the low-order byte of data and third byte specifies the low-order byte of data**

STA 16 bit Addr: Content of accumulator is stored in memory location whose address is specified by 2nd and 3rd byte of instruction.

Opcode	Operand	Byte	M- Cycle	T-State
STA	16 bit	3	4	13

- **No flags are affected.**

LDA 16 bit Addr: Content of memory location memory location whose address is specified by 2nd and 3rd byte of instruction, is loaded in accumulator.

Opcode	Operand	Byte	M- Cycle	T-State
LDA	16 bit	3	4	13

- **No flags are affected.**

STAX Rp: Content of accumulator is copied into memory location whose address is specified by register pair(BC or DE).

Opcode	Operand	Byte	M- Cycle	T-State
STAX	B/D	1	2	7

- **No flags are affected.**

LDAX Rp: Content of memory location whose address is specified by register pair(BC or DE), is loaded in accumulator.

Opcode	Operand	Byte	M- Cycle	T-State
LDAX	B/D	1	2	7

- **No flags are affected.**

SHLD 16 bit Addr: Content of register L is stored in memory location whose address is specified by 2nd and 3rd byte of instruction and content of register H is stored in next memory location.

Opcode	Operand	Byte	M- Cycle	T-State
SHLD	Addr(16 bit)	3	5	16

- **No flags are affected.**

LHLD 16 bit Addr: Content of memory location memory location whose address is specified by 2nd and 3rd byte of instruction, is loaded into register L and content of next location is copied into register H.

Opcode	Operand	Byte	M- Cycle	T-State
LHLD	Addr(16 bit)	3	5	16

- **No flags are affected.**

IN 8 bit addr (Port Address): Accept(read) data byte from an input device and place it in the accumulator.

OUT 8 bit addr (Port Address): Send(write) data byte from the accumulator to an output device.

Opcode	Operand	Byte	M- Cycle	T-State
IN	Addr(8 bit)	2	3	10
OUT	Addr(8 bit)	2	3	10

- **No flags are affected.**

XCHG: Exchange the contents of H-L pair with D-E pair.

Opcode	Operand	Byte	M- Cycle	T-State
XCHG	None	1	1	4

- **No flags are affected.**

SPHL: Copy the contents of H and L register into the stack pointer.

Opcode	Operand	Byte	M- Cycle	T-State
SPHL	None	1	1	6

- **No flags are affected.**

Arithmetic Operations

- **Addition:** Any 8-bit data, or the contents of a register, or the contents of a memory location can be added to the contents of accumulator. Result is stored in accumulator.
- **Subtraction:** Any 8-bit data, or the contents of a register, or the contents of a memory location can be subtracted from the contents of accumulator. Result is stored in accumulator.

  Subtraction is performed in 2's complement.

  No two other 8-bit registers can be added/subtracted directly
- **Increment/decrement:** The content of register/register pair/ memory location can be incremented/decremented by 1.

ADD R/M : Add the content of register or memory location to the content of accumulator.

Result is stored in accumulator.

If second operand is a memory location then it is addressed by HL pair register.

Opcode	Operand	Byte	M- Cycle	T-State
ADD	R	1	1	4
ADD	M	1	2	7

- **All flags are modified.**

ADC R/M : Add the content of register or memory location and the carry bit(flag) to the content of accumulator.

If second operand is a memory location then it is addressed by HL pair register.

. Result is stored in accumulator.

Previous carry flag is reset.

Opcode	Operand	Byte	M- Cycle	T-State
ADC	R	1	1	4
ADC	M	1	2	7

- **All flags are modified.**

ADI 8-bit data : Add the 8 bit immediate data to the content of accumulator.

ACI 8-bit data : Add the 8 bit immediate data and carry bit(flag) to the content of accumulator

Result is stored in accumulator.

Opcode	Operand	Byte	M- Cycle	T-State
ADI	8 bit data	2	2	7
ACI	M	2	2	7

- **All flags are modified.**

SUB R/M : Subtract the content of register or memory location from the content of accumulator.

Result is stored in accumulator.

If second operand is a memory location then it is addressed by HL pair register.

Opcode	Operand	Byte	M- Cycle	T-State
SUB	R	1	1	4
SUB	M	1	2	7

- **All flags are modified.**

SBB R/M : Subtract the content of register or memory location and the carry bit(flag) from the content of accumulator.

If second operand is a memory location then it is addressed by HL pair register.

. Result is stored in accumulator.

Previous barrow(carry) flag is reset.

Opcode	Operand	Byte	M- Cycle	T-State
SBB	R	1	1	4
SBB	M	1	2	7

- **All flags are modified.**

SUI 8-bit data : Subtract the 8 bit immediate data from the content of accumulator.

SBI 8-bit data : Subtract the 8 bit immediate data and carry bit(flag) from the content of accumulator

Result is stored in accumulator.

Opcode	Operand	Byte	M- Cycle	T-State
SUI	8 bit data	2	2	7
SBI	M	2	2	7

- **All flags are modified.**

INR R/M : Increment the content of register or memory location by 1.

If second operand is a memory location then it is addressed by HL pair register.

. Result is stored in register or memory location.

Opcode	Operand	Byte	M- Cycle	T-State
INR	R	1	1	4
INR	M	1	3	10

- **All flags are modified except carry flag.**

DCR R/M : Decrement the content of register or memory location by 1.

If second operand is a memory location then it is addressed by HL pair register.

. Result is stored in register or memory location.

Opcode	Operand	Byte	M- Cycle	T-State
DCR	R	1	1	4
DCR	M	1	3	10

- **All flags are modified except carry flag.**

INX Rp : Increment the content of register pair by 1.

DCX Rp : Decrement the content of register pair by 1.

Result is stored in register pair.

Opcode	Operand	Byte	M- Cycle	T-State
INX	Rp	1	1	6
DCX	Rp	1	1	6

- **No flags are affected.**

DAD Rp : Add the contents of register pair or stack pointer to the contents of HL pair register.

. Result is stored in HL pair register.

Opcode	Operand	Byte	M- Cycle	T-State
DAD	Rp/SP	1	3	10

- **Only carry flag is set when result is larger than 16 bits.**

DAA (Decimal Adjust Accumulator): Converts the contents of the accumulator from a binary value to two 4 bit binary coded decimal(BCD) digit.

- **All flags are modified.**