VLSI Design (BEC-41)
(Unit-1, Lecture-1)

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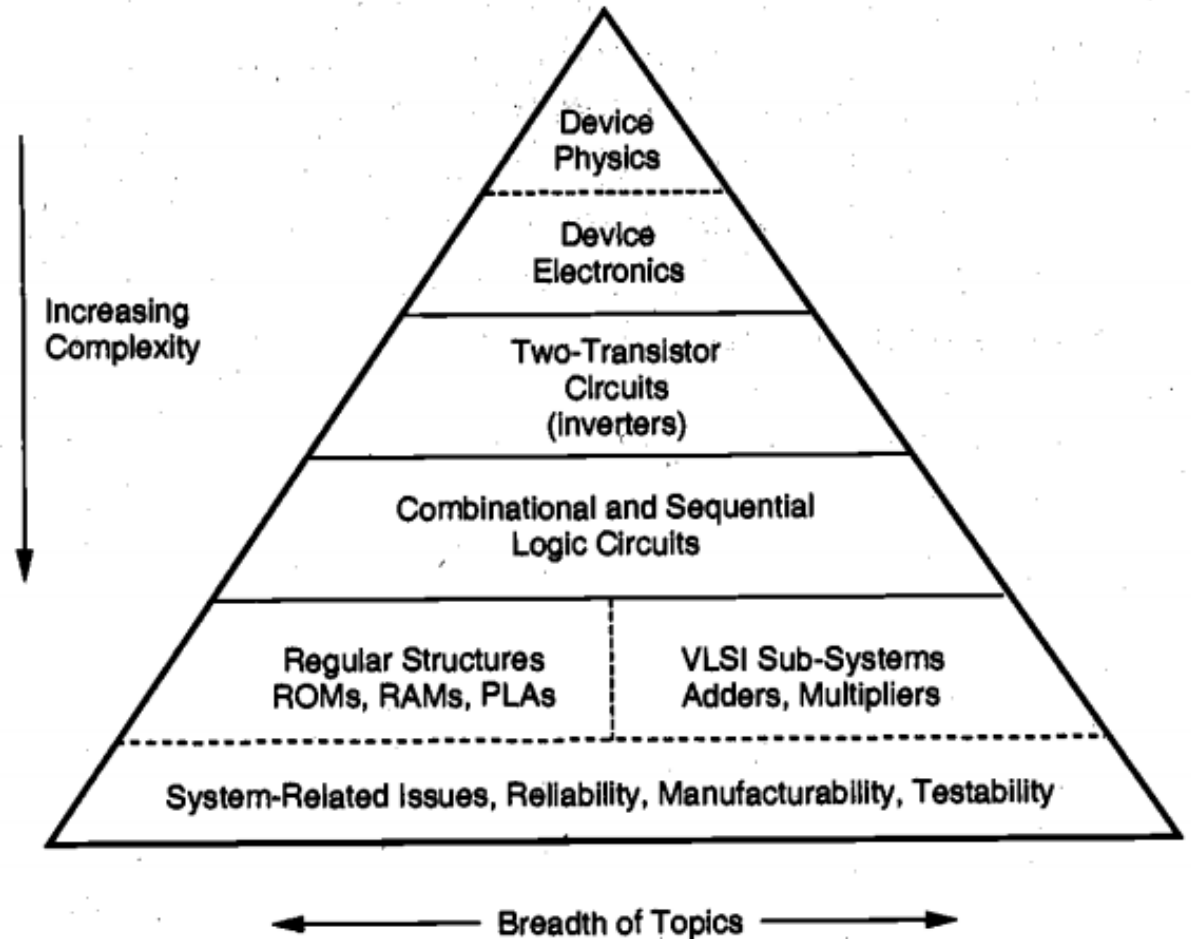
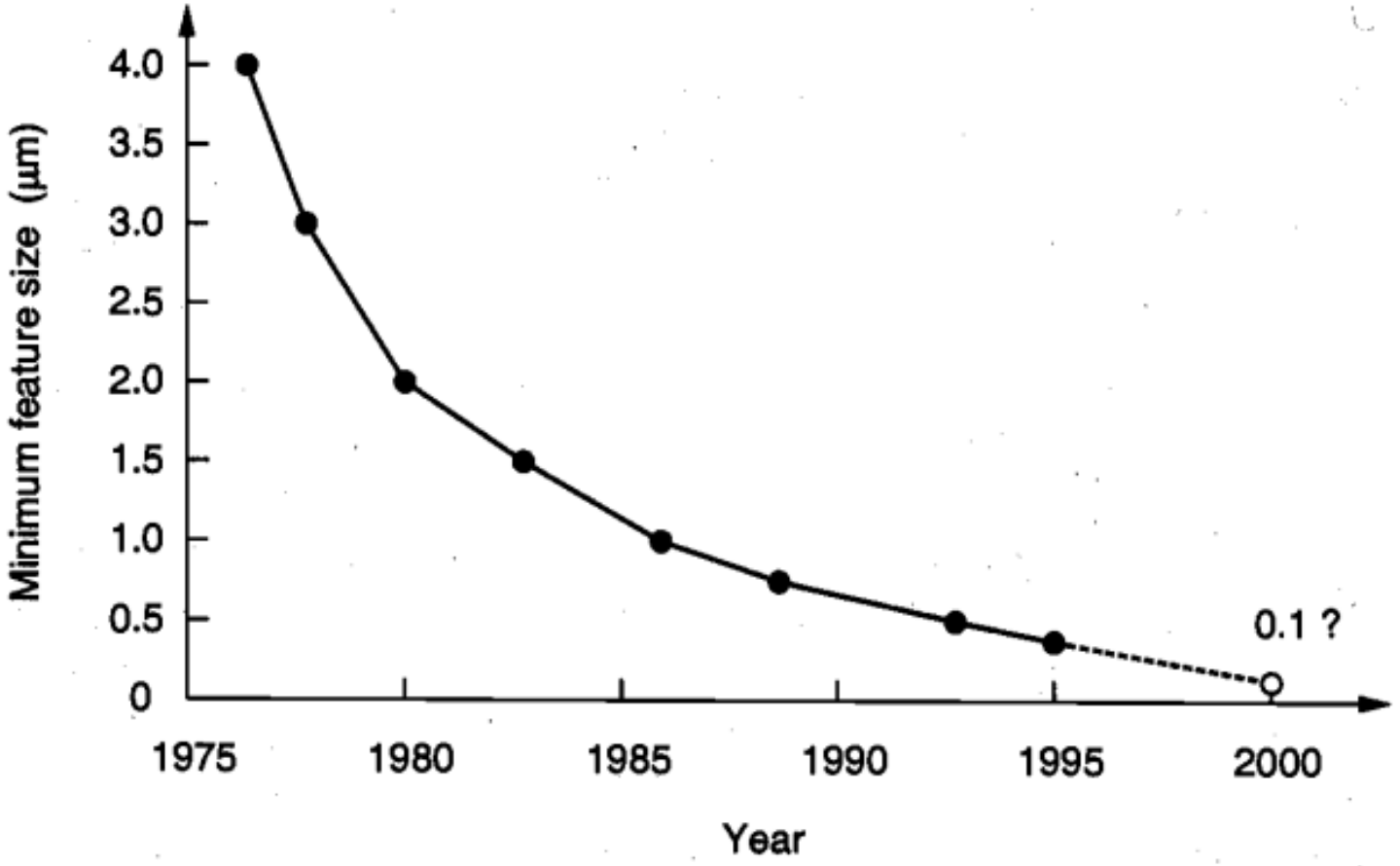
Outcomes

- **Trends & Projections in VLSI Circuits**
- **Flow diagram of VLSI Circuit Design**
- **VLSI Design issues**
- **Y-Chart**

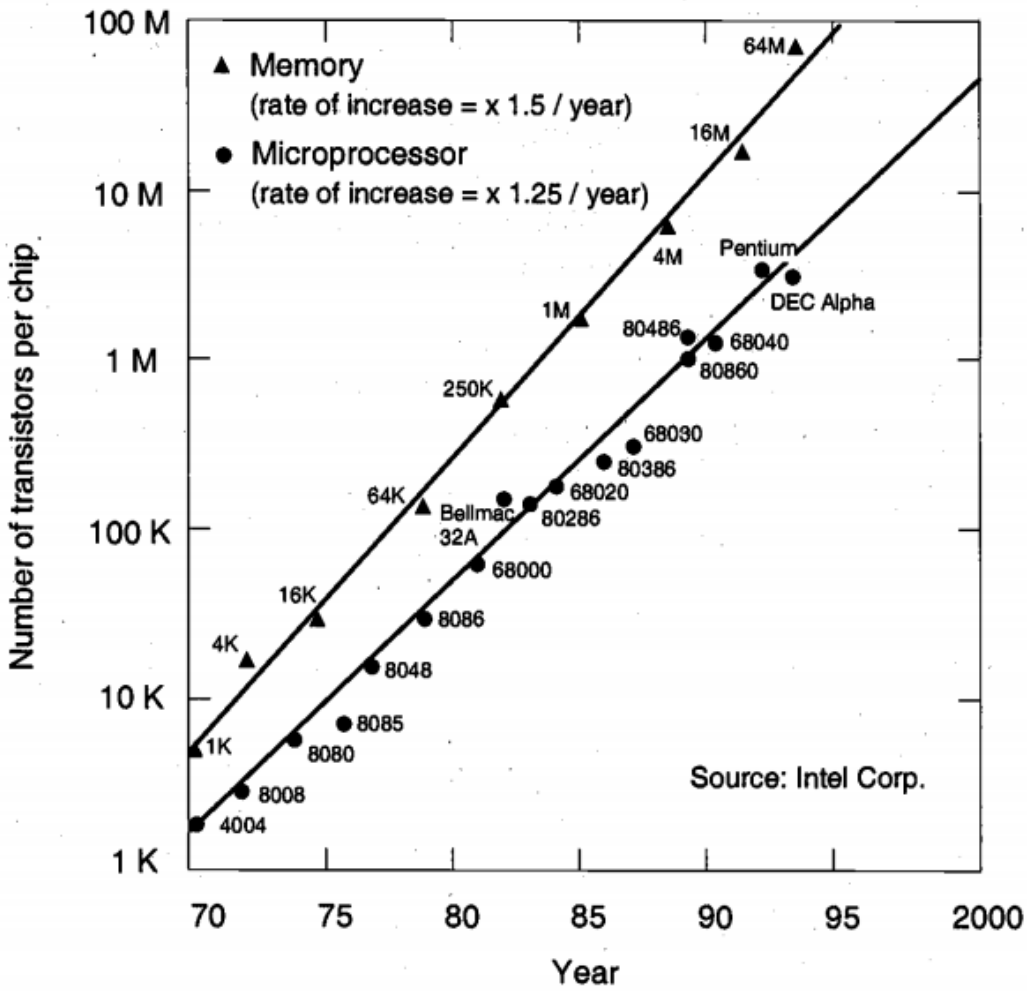
The ordering of topics covered in a typical digital integrated circuits course



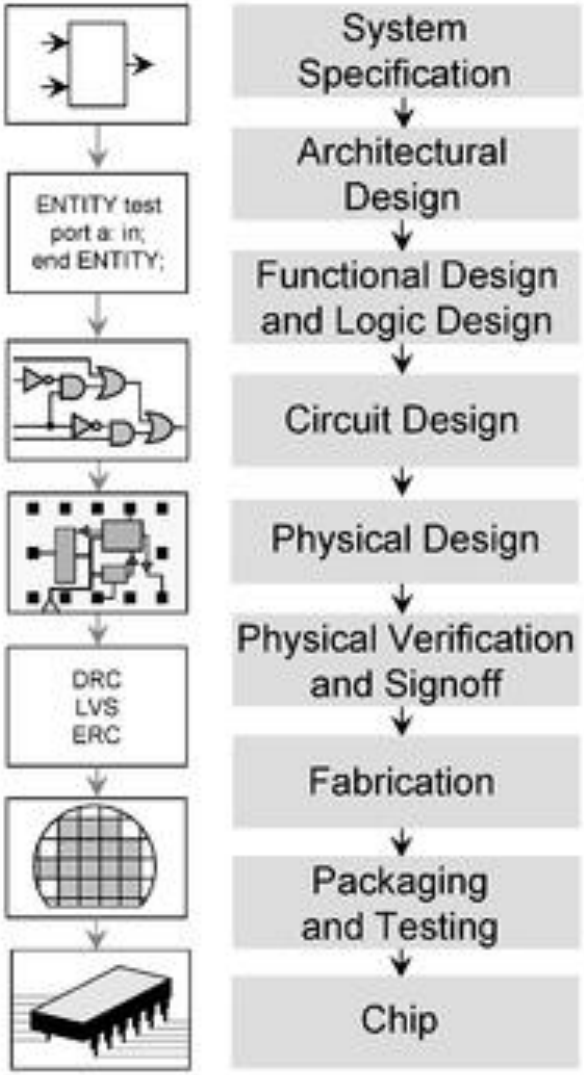
Evolution of minimum feature size in integrated circuits over time



Level of integration versus time for memory chips and logic chips

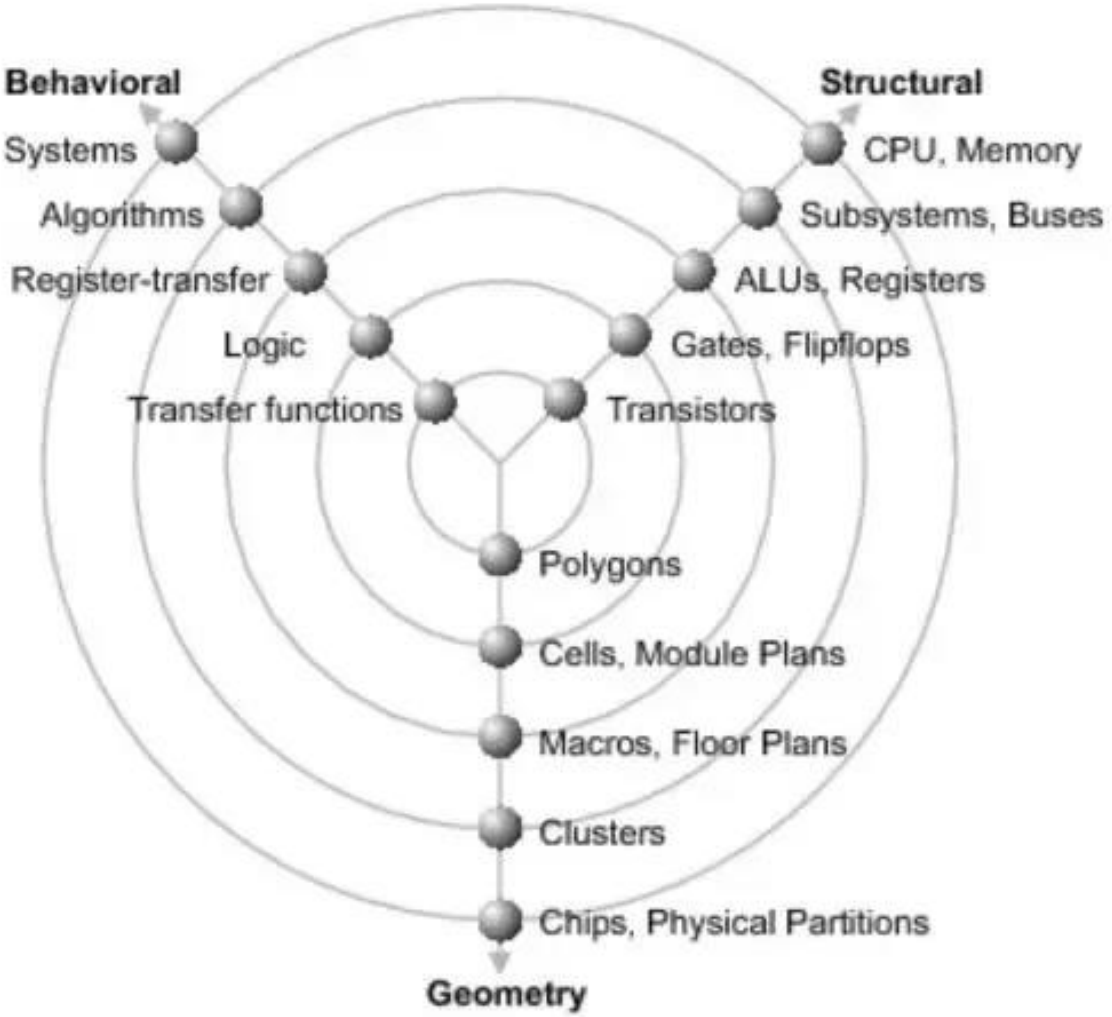


VLSI Design Flow



- Specifications comes first, they describe abstractly, the functionality, interface, and the architecture of the digital IC circuit to be designed.
- Behavioral description is then created to analyze the design in terms of functionality, performance, compliance to given standards, and other specifications.
- RTL description is done using HDLs. This RTL description is simulated to test functionality. From here onwards we need the help of EDA tools.
- RTL description is then converted to a gate-level netlist using logic synthesis tools. A gate level netlist is a description of the circuit in terms of gates and connections between them, which are made in such a way that they meet the timing, power and area specifications.
- Finally, a physical layout is made, which will be verified and then sent to fabrication.

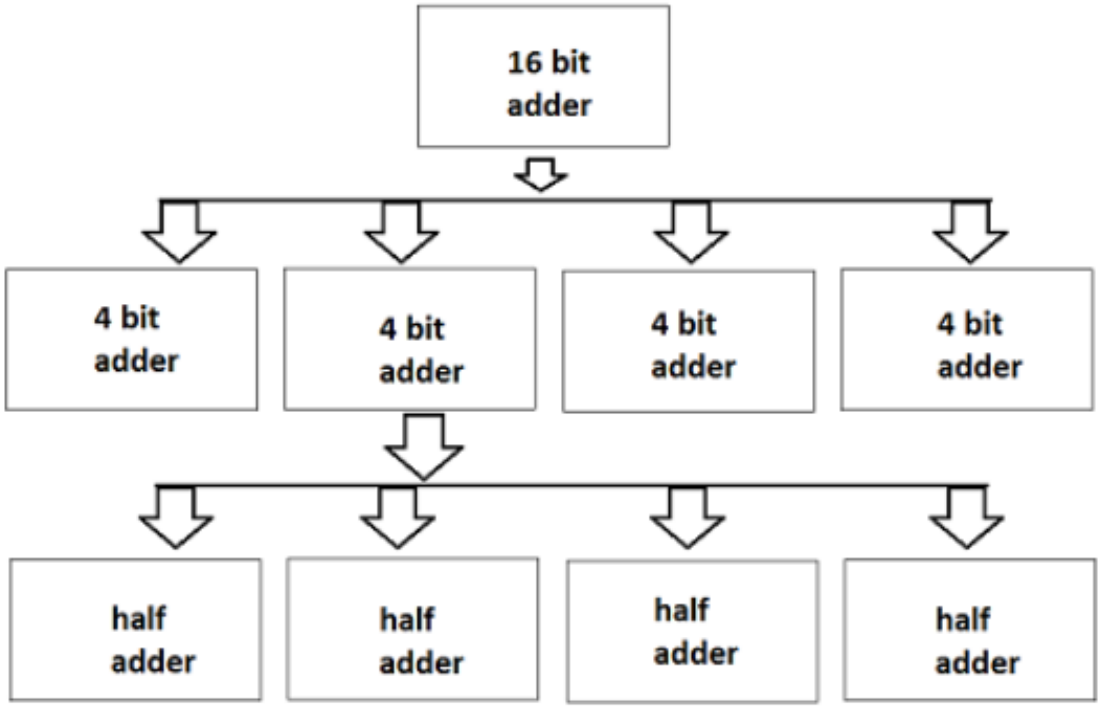
Y-Chart



- The Gajski-Kuhn Y-chart is a model, which captures the considerations in designing semiconductor devices.
- The three domains of the Gajski-Kuhn Y-chart are on radial axes. Each of the domains can be divided into levels of abstraction, using concentric rings.
- At the top level (outer ring), we consider the architecture of the chip; at the lower levels (inner rings), we successively refine the design into finer detailed implementation
- Creating a structural description from a behavioral one is achieved through the processes of high-level synthesis or logical synthesis.
- Creating a physical description from a structural one is achieved through layout synthesis.

Design Hierarchy-Structural

- The design hierarchy involves the principle of "Divide and Conquer." It is nothing but dividing the task into smaller tasks until it reaches to its simplest level. This process is most suitable because the last evolution of design has become so simple that its manufacturing becomes easier.
- We can design the given task into the design flow process's domain (Behavioral, Structural, and Geometrical). To understand this, let's take an example of designing a 16-bit adder, as shown in the figure below.



Concepts of Regularity, Modularity and Locality

The hierarchical design approach reduces the design complexity by dividing the large system into several sub-modules. Usually, other design concepts and design approaches are also needed to simplify the process.

- **Regularity** means that the hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. A good example of regularity is the design of array structures consisting of identical cells - such as a parallel multiplication array.
- **Modularity** in design means that the various functional blocks which make up the larger system must have well-defined functions and interfaces. Modularity allows that each block or module can be designed relatively independently from each other, since there is no ambiguity about the function and the signal interface of these blocks. All of the blocks can be combined with ease at the end of the design process, to form the large system. The concept of modularity enables the parallelization of the design process. It also allows the use of generic modules in various designs - the well-defined functionality and signal interface allow plug-and-play design.
- The concept of **locality** also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible. This last point is extremely important for avoiding excessive interconnect delays. Time-critical operations should be performed locally, without the need to access distant modules or signals. If necessary, the replication of some logic may solve this problem in large system architectures.

VLSI Design Style